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GreenMil International

Quality Team

# [PCB LAYOUT DESIGN GUIDELINES CHECKLIST]

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# PCB Layout Design Guidelines

# Revision History

| Version | Date | Author | Remarks | Approved by |
|---|---|---|---|---|
| 1.0 | 26/04/2007 | Lloyd K Das | | |
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GMI/CAD/01/Rev 1.0

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# 1. Component Creation

1.1 Measurement unit mils are to be used for any dimension used for component creation. Dimensions given in mm are to be converted to mils by multiplying it 39.37 and has to be rounded of to two decimal places.

1.2 Origin of the component created has to be at its body center.

1.3 If given, use the footprint dimensions provided by the manufacturer from the datasheet.

1.4 From the datasheet consider the 'nominal' dimensions if minimum, maximum and nominal dimensions are provided.

1.5 Drill size for through hole components have to be actual pin size + 14 mils. The final drill size has to be divisible by 2 else round of to the next higher value which is divisible by 2.

1.6 For press fit connectors use the recommended value provided by the manufacturer.

1.7 Through hole pad size should be final drill size + 25 mils and should be rounded of to 0 decimal places. However the value of 25 mils can be reduced to 20 mils for smaller pads

1.8 For plated through hole pads both thermal pads and antipads have to be provided.

1.9 Thermal pads have to be defined as flash and the naming convention should be F(thermal outer pad dia)X(thermal inner pad dia)X(spoke width) E.g. F90X70X25

1.10 Anti pad size should be 20 mils + pad size

1.11 For NPTH drills, minimum antipad and route keep out of 20 mils+drill size should be defined.

1.12 Thermal relief spoke width should be a minimum of 20 mils.

1.13 For through hole components pin 1 should always be a square pad.

1.14 The inner pad of the thermal relief should be 20 mils + the pad size.

1.15 The outer pad of the thermal relief should be inner pad diameter + 20 mils. E.g. In the datasheet if the actual pin dia is 25 mils then, Drill size = 25+14=39. Rounded of to 40 mils. Pad size = 40 + 25=65 mils. Thermal relief inner pad = 65+20=75. Outer pad size = 75+20=95 and anti pad size = 65+20=75. Flash=F95X75X20

1.16 Solder mask of minimum 6 mil + pad size should be provided for all through hole and smd pads except for BGA.

1.17 No solder mask opening is to be provided on the top layer for escape vias used in a BGA.

1.18 For through hole pads solder mask should be provided on both top and bottom layers.

1.19 For pads used in BGA solder mask should be same as pad size.

1.20 Paste mask should be same as pad size for smd pads.

1.21 Line width used for component outlines/assembly outlines has to be a minimum of 7 mils.

1.22 Silk screen outline for BGA should be exactly same as the actual body outline of the BGA.

1.23 Silk screen outline for other devices can be 10 mil + actual body outline.

1.24 Polarity markings should be provided for polarized components such as Tantalum/Electrolytic capacitors, Diodes etc. A '+" marking is to be given at pin 1 for all polarized capacitors and a diode symbol for all diodes with pin 1 as anode.

1.25 A placement boundary of Silk screen outline + 15 mils (minimum) is to be provided for all components on the top layer. For BGA's this value has to be Silk screen outline + 100 mils.

1.26 Direction marking arrows should be provided on silk screen for right angled connectors/Switches or other components which are placed at the edge of the board and which are to be accessed from outside.

1.27 A filled circle of radius 10 mils is to be provided as pin 1 marking for all components on both silk screen and assembly.

1.28 Corner pin numbers in text to be marked on both silk screen and assembly for components having pin count > 2.

1.29 For larger pin count devices pin number markings are to be provided on silkscreen at standard repetitions. Preferably after every 10 pin for components having pin count > 30

1.30 Reference Designators have to be placed on both Assembly and silk screen Layers. In the Assembly layer the reference designators have to be placed in the component body center.

1.31 The text size used for reference designator has to be 'Text size 3' and having values: Width=25, Height=35, Line spacing= 60 Photo plot width =7 & character spacing=5.

1.32 The text size used for pin no. markings has to be 'Text size 2' and having values: Width=23, Height=32, Line spacing= 30 Photo plot width =6 & Character spacing=5.

1.33 Two Local Fiducials have to be placed diagonally for fine pitched components such as BGA's.

1.34 The dimensions of the created component have to be marked in the 'Dimension' subclass and names of the footprints used have to be entered in the 'Pad_stack_layer' subclass of Package geometry.

1.35 The created components have to be added to Dexce_Allegro_library only after it is checked and verified using the PCB Component creation Checklist.

## 2. Placement

2.1 Thickness of the board outline in the Class Board Geometry has to be 10 mils.

2.2 A component keep in area of 75 to 100 mils from the board edge have to be defined in the Area-Component Keep in Subclass.

2.3 Similarly a Route keep in area of 50 mil from the board edge have to be defined in the Area – Route Keep In Subclass.

2.4 All the position critical components or components for which placement is fixed such as Board edge connectors, B to B connectors etc. have to be placed first.

2.5 A minimum of 3 fiducials have to be placed on the top layer and bottom layer. (if components are present in the Bottom layer)

2.6 The Fiducials have to be placed in such a way that they form a right angle triangle.

2.7 Component outlines should not overlap each other.

2.8 Component body outline on bottom layer should not overlap through hole pads.

2.9 Components have to be placed as per the design flow.

2.10 Crystals and oscillator circuits have to be placed close to the respective ICs for which it is meant.

2.11 Decaps have to be placed close to the supply pins of their respective IC's.

2.12 While placing decaps for BGA's, smaller value decaps have to be placed closest to the BGA and then the higher value caps.

2.13 All series termination resistors at the source should be placed as close as possible to the IC

2.14 All parallel terminations should be placed close to the destination.

2.15 In a mixed signal design care must be taken while placing. There should not be any mix up between analog and digital sections.

2.16 Ideally power supply circuitry has to be placed on one corner of the board and should be away from high frequency devices.

## 3. Routing

3.1 Minimum via size used should be 20/10.

3.2 Minimum trace width should be 5 mils for outer layers and 4 mils for inner layers. However, from the cost point of view minimum 6 mil trace width is preferred.

3.3 Minimum trace to trace and trace to pad clearance have to be 5 mils.

3.4 Critical signals and clocks should be routed first then the length matched signals.

3.5 There should not be any unwanted bends on the traces and should be as straight as possible.

3.6 While routing same net DRC must be on.

3.7 There should not be direct short between pads with the same signal. Instead, traces have to be got out of the pin and shorted.

3.8 All power traces that are routed have to be thick.

3.9 Tolerance for length matched differential pair routes is 25 mils.

3.10 There should not be any traces/vias under Crystals/oscillators.

3.11 Memories should be always be routed be in daisy chain.

3.12 Multiple vias are to be used while connecting Power/Gnd to planes from the power source.

3.13 3w space is to be maintained between same trace while serpentine routing.

3.14 All traces have to be mitered and there should not be any 90 degree bends.

3.15 In split planes the copper to copper spacing has to be a minimum of 20 mils. 30 mils are recommended.

3.16 All dangling routes / vias have to be removed after routing.

3.17 As far as possible power supply should be routed as planes.

3.18 A DRC has to be performed on the board before Gerber generation.

# 4. Gerber Generation

4.1 The following film option settings have to be made before generating the gerber.

a. Rotation and offset for all films should be 0.
b. Undefined line width should be 7 mils.
c. Shape bounding box should be 200 mils.
d. Plot mode should be positive for all films except power planes which have to be negative.
e. 'Suppress unconnected pads' should be selected for all power planes.
f. 'Check database before artwork' has to be selected for all films.
g. In the 'General parameters' Device type selected should be 'Gerber RS274x' and format should 5,5.

4.2 A Film name template has to be placed in the Manufacturing → Drawing Format → Title_Data Sub class and should be visible in all films with the film names entered in their respective layers.

4.3 Naming format for the Gerber files have to be: board name_ver No._film name.art. E.g. 'ipsm_v1_bottom.art'

4.4 A readme.doc has to be created with the film details and has to be sent along with the Gerber files for fabrication.

**Sample read me file**:

**FILE DESCRIPTION**

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ipsm_v1_gerber.ZIP - ZIP FILE

**GERBER FILE**

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1. ipsm_v1_top.art - TOP LAYER
2. ipsm_v1_bottom.art - BOTTOM LAYER
3. ipsm_v1_slktop.art - TOP LAYER SILK SCREEN
4. ipsm_v1_slkbot.art - BOTTOM LAYER SILK SCREEN
5. ipsm_v1_smktop.art - TOP LAYER SOLDER MASK
6. ipsm_v1_smkbot.art - BOTTOM LAYER SOLDER MASK
7. ipsm_v1_vcc2.art - PLANE1 (PWR)
8. ipsm_v1_gnd5.art - PLANE2 (GND)
9. ipsm_v1_sig3.art - MID LAYER 1
10. ipsm_v1_sig4.art - MID LAYER 2

11. ipsm_v1_sig6.art - MID LAYER 3
12. ipsm_v1_sig7.art - MID LAYER 4
13. ipsm_v1_pmtop.art - TOP LAYER PASTE MASK
14. ipsm_v1_pmbot.art - BOTTOM LAYER PASTE MASK

**NC DRILL DATA**

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1. ipsm_v1_nc.drl - DRILL DATA
2. ipsm_v1_ncdrill.txt - DRILL TOOL REPORT (TEXT FILE)
3. ipsm_v1_drilldwg.art - DRILL DRAWING

**PICK & PLACE REPORT (FOR ASSEMBLY HOUSE ONLY)**

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ipsm_v1_pik-place.txt

IPC-D-356 NETLIST

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ipsm_v1_IPCD356.ipc

**LAYERING INFORMATION**

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LAYER1 - ipsm_v1_top.art
LAYER2 - ipsm_v1_vcc2.art (PWR PLANE)
LAYER3 - ipsm_v1_sig3.art
LAYER4 - ipsm_v1_sig4.art
LAYER5 - ipsm_v1_gnd5.art (GND PLANE)
LAYER6 - ipsm_v1_sig6.art
LAYER7 - ipsm_v1_sig7.art
LAYER8 - ipsm_v1_bottom.art

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**FABRICATION INSTRUCTION**

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P/N :
QTY :
MAT : FR-4 1.6MM
CU : 35 MICRONS
PROCESS : HOT AIR LEVELING
FINISH : 2 SIDES WITH SOLDER MASK 2 SIDES WITH LEGEND (WHITE)
OTHERS : CNC ROUTING FOR BOARD OUTLINE
FULL ELECTRICAL TEST (FOR OPEN/SHORT)