2009

GreenMil International

Quality Team

[PRE FABRICATION PCB DESIGN JOB WORK CHECKLIST]

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Pre Fabrication PCB Checklist

Date:

Board Name/Part No.				**Rev**		**Project**	
Ckt Designer				**Layout Designer**			
No. of layers		**Material**		**Impedance Controlled**		**Thickness**	

Sl. No.	Description	Status
1.	Check the physical dimensions of the board. (For boards that follow any particular standard eg. PCI, VME etc. or, if provided by the customer)	
2.	Crosscheck the component packages used on the board with the BOM	
3.	Ensure that all the components used have been checked as per PCB Component creation checklist.	
4.	Check if Component keep in area of 100 mil from edge of the board have been provided for Top and Bottom layers	
5.	Check if Route keep in area of 50 mil from edge of the edge of the board have been provided for all layers	
6.	Ensure that sufficient mounting holes have been provided for stand alone boards.	

7.	Check the diameters of the mounting holes provided	
8.	Check if a clearance of 100 mil has been provided surrounding the mounting hole	
9.	Check if a minimum of 3 fiducials marks have been placed on Top & Bottom (if components are present) layers.	
10.	Check if all fine pitched components have local fiducials.	
11.	Check if clearance areas of 100 mils have been provided on the Top Layer surrounding the BGA for rework. However, this rule can be compromised with any components below 1206 package for highly dense boards.	
12.	Check the orientation of all the Rt angled connectors/switches that are at the board edge.	
13.	Check if there is any accidental overlapping of components.	
14.	In case of components being mounted on both the sides, check if components overlap through hole solder pads of the opposite layer.	
15	Check if there is sufficient clearance between components.	
16.	Check the placement of critical components like connectors, crystals, oscillators etc.	
17.	Check the placement of Decaps. Ensure that they are placed close to the power pins of their respective IC's.	
18.	Check the placement of Berg stick & headers. Ensure that they can be accessed easily and do not hinder accessibility of other components.	
19.	Check if all components have been placed and routing completion is100%	
20.	Check for any traces or vias under Oscillators and crystals.	

21.	Check the routing of Critical signals given as per the routing guidelines for the Board	
22.	Check the routing of differential traces. Ensure that both the traces are parallel and are equidistant to each other from source to destination	
23.	Check for any dangling traces and vias.	
24.	Check if all the traces have been mitered and there are no 90° bends.	
25.	Check the power planes and ensure that anti pad size is a min of 15mil + actual pad size.	
26.	Check if thermal pads have been provided for all through hole components connected to the plane.	
27.	Check if the vias used for fanning out the BGA are fully connected in the plane.	
28.	Check if all the vias have been masked on both the Top and Bottom layers	
29.	For split power planes the split or the copper to copper spacing has to be a minimum of 20 mils. 30 mils are recommended.	
30.	Check if there is sufficient enough connectivity for the pads/vias in the split plane	
31.	Check if test points have been provided for Power supply signals and are marked on the silkscreen	
32.	Check if sufficient test points have been provided for Gnd signal and are distributed evenly across the board	
34.	Check if Polarity indication have been given for all polarized components like Diodes Capacitors etc.	
35.	Check the polarity of all the polarized capacitors and ensure that the polarity markings are correct.	

36.	Check the polarity of all the Diodes and ensure that the polarity markings are correct.	
37.	Check the positions of all the ref designators. Ensure that they are placed close to their respective components and are not interchanged.	
38.	Check that the ref designators/legend markings are not placed on component pads/vias and are legible	
39.	Ensure that the text size used for ref Designators is 'Text Size 3' having values: Width=25, Height=35 Line spacing=60 Photo plot width=7 & char spacing=5	
40.	Ensure that the text size used for pin nos. is 'Text Size 2' having values: Width=23, Height=32 Line spacing=30 Photo plot width=6 & char spacing=5	
41.	Ensure that the text size used for all other silk screen texts is 'Text Size 4' having values: Width=35, Height=45 Line spacing=60 Photo plot width=7 & char spacing=5	
42.	Check if Company Name and Logo have been placed on the top silk screen layer.	
43.	Check if Layer identification no. has been provided on all layers and 'Text Size 4' is used.	
44.	Check if Board Name/Revision has been placed on the Top layer. (Board Name/Revision has to be placed in the bot layer only if the top layer is quite dense and there is no space.)	
45.	Ensure that the text size used for Board Name/Revision is 'Text Size 4' having values: Width=35, Height=45 Line spacing=60 Photo plot width=7 & char spacing=5	
46	Check if all the text on Bot silk screen layer is mirrored.	
47	Check if the data entered in the title block for film identification are correct and the text size used is 'Text Size 5' having values: Width=117, Height=156 Line spacing=195 Photo plot width=12 & char spacing=60	
48.	Perform a DRC on the board and ensure that there are no errors	

49.	Make sure that all the Pcb Design Checklist / guidelines are strictly followed. There can be some exceptions in some cases. But these have to be well documented before deviation.	

Checked By

Verified By

Date:

Date: